SiT9103

LVPECL / HCSL / LVDS / CML
3-PLL High Performance Clock Generator

Features

- Extremely low RMS phase jitter (random)
  - <1 ps (typical)
- Wide frequency range
  - 1 MHz to 220 MHz
  - 220 MHz to 800 MHz (contact SiTime)
- Three independent PLLs
- Low frequency tolerance
  - ±25 PPM or ±50 PPM
- Operating voltage
  - CML: 1.8, 2.5 or 3.3 V
  - LVPECL/LVDS: 2.5 or 3.3 V
  - Other voltages up to 3.63 V (contact SiTime)
- Operating temperature range:
  - Industrial, -40 to 85°C
  - Extended Commercial, -20 to 70°C
- Small footprint
  - 22-pin, 7.0 x 5.0 x 0.9 mm QFN package
- All packages are Pb-free and ROHs compliant
- Ultra-reliable start up and greater immunity from interference

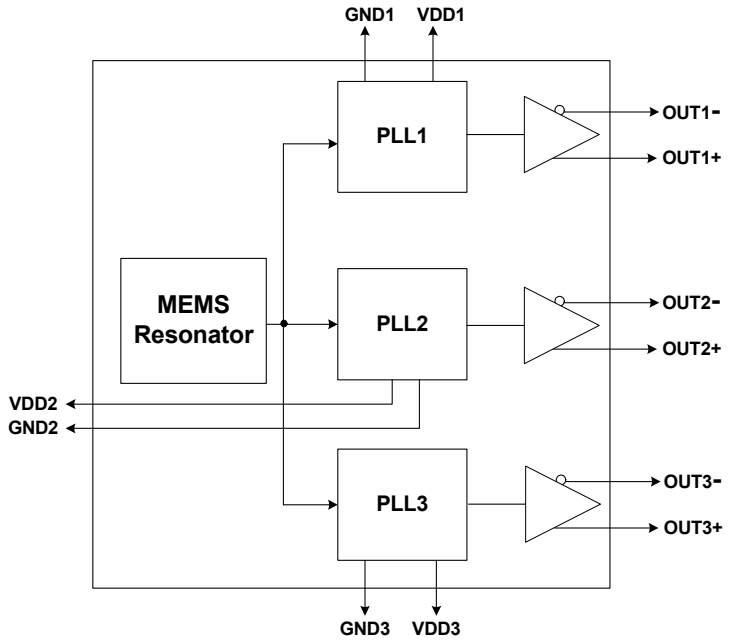
Benefits

- Replacing up to three differential clock output oscillators
- Integrated resonator
- No crystal or load capacitors required
- Eliminates crystal qualification time
- 50% + board saving space
- More cost effective than quartz oscillators, quartz crystals and clock ICs.
- Completely quartz-free

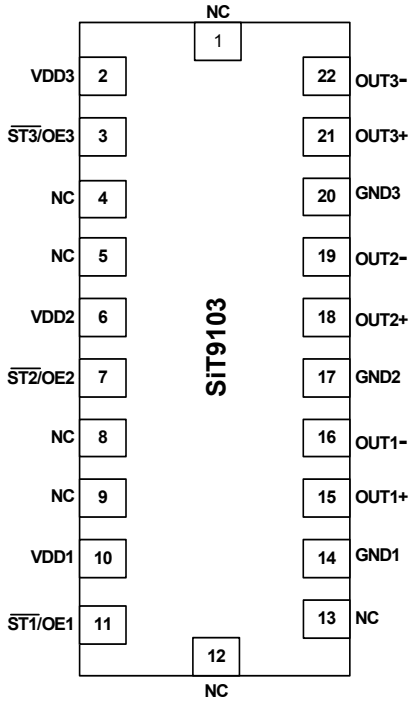
Applications

- Server
- Router
- RAID controller
- Gigabit Ethernet
- 10 Gigabit Ethernet
- Fiber Channel
- SATA / SAS
- PCI-Express
- System clock
- Networking and computing

Block Diagram



Pinout



Pin Description

Pin No.	Name	Pin Description
1,4, 5, 8,9,12,13	NC	Do Not connect pins, leave them floating
2	VDD3	Power supply for OUT3+ and OUT3- Connect to 2.5V or 3.3V for LVPECL/ HCSL/ LVDS and 1.8V or 2.5V or 3.3V for CML
3	$\overline{ST3}$/OE3	Standby or Output Enable pin for OUT3+ and OUT3-
6	VDD2	Power supply for OUT2+ and OUT2-. VDD2 must be on all times for porper operation Connect to 2.5V or 3.3V for LVPECL/ HCSL/ LVDS and 1.8V or 2.5V or 3.3V for CML
7	$\overline{ST2}$/OE2	Standby or Output Enable pin for OUT2+ and OUT2- $\overline{ST2}$ = 0, the resonator will be disabled (do not use unless the whole chip is going to ST mode) $\overline{ST2}$ = 1, PLL1, PLL2 and PLL3 will operate normally
10	VDD1	Power supply for OUT1+ and OUT1-. Connect to 2.5V or 3.3V for LVPECL/ HCSL/ LVDS and 1.8V or 2.5V or 3.3V for CML
11	$\overline{ST1}$/OE1	Standby or Output Enable pin for OUT1+ and OUT1-
14	GND1	Power supply ground. Connect to Ground
15,16	OUT1+, OUT1-	1 to 220 MHz programmable differential clock output pair at VDD1 level (LVPECL/ HCSL/ LVDS = 2.5V or 3.3V, CML = 1.8V or 2.5V or 3.3V)
17	GND2	Power supply ground. Connect to Ground
18, 19	OUT2+, OUT2-	1 to 220 MHz programmable differential clock output pair at VDD2 level (LVPECL/ HCSL/ LVDS = 2.5V or 3.3V, CML = 1.8V or 2.5V or 3.3V)
20	GND3	Power supply ground. Connect to Ground
21, 22	OUT3+, OUT3-	1 to 220 MHz programmable differential clock output pair at VDD3 level (LVPECL/ HCSL/ LVDS = 2.5V or 3.3V, CML = 1.8V or 2.5V or 3.3V)

Pins 3,7,11

Pin #s 3,7,11 Functionality
OE (3,7,11)
H or Open; specified frequency output
L: output is high impedance
$\overline{ST}$ (3,7,11)
H or Open; specified frequency output
L: output is low level (weak pull down) oscillation stops

Description

The SiT9103 is a 3-PLL factory programmable clock generator with embedded MEMS resonator. The device uses SiTime propriety MEMS technology, MEMS First™, to enable a single chip solution with multiple outputs for consumer and communications applications.

The SiT9103 has three PLLs that can be programmed to generate any frequency outputs from 1 to 220 MHz .

Each PLL is connected to one differential output buffer that can generate a single differential output frequency at LVPECL, LVDS, CML, or HCSL signalling.

Programming Configuration

The SiT9103 is a factory programmable device. All the parameters in table 1 given as “Enter Data” can be programmed into the device.

Table 1.

	PLL1					PLL2					PLL3				
Pin Name	OUT1[+,-] 1- 220MHz	$\overline{ST1}$/ OE1	VDD1 1.8/2.5/3.3V	Signaling Type (LVPECL / LVDS / CML / HCSL	Swing Mode (Normal / High)	OUT2[+,-] 1- 220MHz	OE2	VDD2 1.8/2.5/3.3V	Signaling Type (LVPECL/ LVDS/, CML/HCSL	Swing Mode (Normal / High)	OUT3[+,-] 1- 220MHz	$\overline{ST3}$/ OE3	VDD3 1.8/2.5/3.3V	Signaling Type (LVPECL/ LVDS/ CML/HCSL	Swing Mode (Normal / High)
Pin No.	15,16	11	10			18,19	7	6			21,22	3	2		
Program Value	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”	“Enter Data”

Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Absolute Maximum Table

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	+4.00	V
Theta JA (with copper plane on VDD and GND)	–	27.5	°C/W
Theta JC (with PCB traces of 0.010 inch to all pins)	–	47	°C/W
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Number of Program Writes	–	1	NA
Program Retention over -40 to 125 °C, Process, VDD (0 to 3.6V)	–	1,000+	years
Human Body Model (JESD22-A114)	2000	–	–
Charged Device Model (JESD22-C101)	750	–	–
Machine Model (JESD22-A115)	200	–	–

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	MIL-STD-883F, Method 1010-65-150°C (1000 cycle)
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1

DC Electrical Specifications

LVCMOS input, OE or ST pin, 3.3V ±10% or 2.5V ±10% or 1.8V ±5%, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage		70	–	–	%Vdd
V_{IL}	Input Low Voltage		–	–	30	%Vdd
I_{IH}	Input High Current	OE or ST pin	–	–	10	µA
I_{IL}	Input Low Current	OE or ST pin	-10	–	–	µA

LVPECL, 3.3V ±10% or 2.5V ±10%, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
I_{DD}	Supply Current	V_{DD2} = 3.3V or 2.5V, OUT2[+,-] = active	–	68	74	mA
		$V_{DD1} = V_{DD3} = 0V$ (Exluding Load Termination Current)	–	65	71	mA
V_{OH}	Output High Voltage	50 Ohm termination to V_{DD} - 2.0V	V_{DD}-1.1	–	V_{DD}-0.7	V
V_{OL}	Output Low Voltage	See Figure 2, 3.	V_{DD}-2.0	–	V_{DD}-1.4	V
V_{swing}	Pk-PK Output Voltage Swing		600	800	1000	mV

HCSL, 3.3V ±10% or 2.5V ±10%, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
I_{DD}	Supply Current	V_{DD2} = 3.3V or 2.5V, OUT2[+,-] = active	–	65	70	mA
		$V_{DD1} = V_{DD3} = 0V$ (Exluding Load Termination Current)	–	62	67	mA
V_{OH}	Output High Voltage	50 Ohm termination to GND	0.6	0.75	0.95	V
V_{OL}	Output Low Voltage	See Figure 4.	0.0	–	0.50	V
V_{swing}	Pk-PK Output Voltage Swing		600	750	950	mV

LVDS, 3.3V ±10% or 2.5V ±10%, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
I_{DD}	Supply Current	V_{DD2} = 3.3V or 2.5V, OUT2[+,-] = active	–	73	79	mA
		$V_{DD1} = V_{DD3} = 0V$ (Exluding Load Termination Current)	–	70	76	mA
V_{OD1}	Differential Output Voltage	Swing Mode = Normal	250	350	450	mV
ΔV_{OD1}	V_{OD} Magnitude Change	Single load termination.	–	–	50	mV
V_{OS1}	Offset Voltage	See Figure 5.	–	1.2	–	V
ΔV_{OS1}	V_{OS} Magnitude Change		–	–	50	mV
V_{OD2}	Differential Output Voltage	Swing Mode = High	500	700	900	mV
ΔV_{OD2}	V_{OD} Magnitude Change	Single load termination.	–	–	50	mV
V_{OS2}	Offset Voltage	See Figure 5.	–	1.2	–	V
ΔV_{OS2}	V_{OS} Magnitude Change		–	–	50	mV
V_{OD3}	Differential Output Voltage	Swing Mode = High	250	350	450	mV
ΔV_{OD3}	V_{OD} Magnitude Change	Double load termination.	–	–	50	mV
V_{OS3}	Offset Voltage	See Figure 6.	–	1.2	–	V
ΔV_{OS3}	V_{OS} Magnitude Change		–	–	50	mV

CML, 3.3V ±10% or 2.5V ±10% or 1.8V ±5%,-40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.89	V
I_{DD}	Supply Current	V_{DD2} = 3.3V or 2.5V, OUT2[+,-] = active V_{DD1} = V_{DD3} = 0V (Exluding Load Termination Current)	–	48	51	mA
		V_{DD2} = 3.3V or 2.5V, OUT2[+,-] = active V_{DD1} = V_{DD3} = 0V (Exluding Load Termination Current)	–	47	50	mA
		V_{DD2} = 3.3V or 2.5V, OUT2[+,-] = active V_{DD1} = V_{DD3} = 0V (Exluding Load Termination Current)	–	38	41	mA
V_{OH1}	Output High Voltage	Swing Mode = Normal Single Load Termination See Figure 7.	V_{DD}-0.1	–	V_{DD}	V
V_{OL1}	Output Low Voltage		V_{DD}-0.55	V_{DD}-0.425	V_{DD}-0.3	V
V_{swing1}	Pk-PK Output Voltage Swing		300	425	550	mV
V_{OH2}	Output High Voltage	Swing Mode = High Single Load Termination See Figure 7.	V_{DD}-0.1	–	V_{DD}	V
V_{OL2}	Output Low Voltage		V_{DD}-1.1	V_{DD}-0.85	V_{DD}-0.6	V
V_{swing2}	Pk-PK Output Voltage Swing		600	850	1100	mV
V_{OH3}	Output High Voltage	Swing Mode = High Double Load Termination See Figure 8.	V_{DD}-0.1	–	V_{DD}	V
V_{OL3}	Output Low Voltage		V_{DD}-0.55	V_{DD}-0.425	V_{DD}-0.3	V
V_{swing3}	Pk-PK Output Voltage Swing		300	425	550	mV

AC Electrical Specifications

LVPECL, 3.3V ±10% ,-40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{sta}	Frequency Stability	Inclusive of initial tolerance, operating temperature, rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	PPM
			-40 to 85°C	-50	–	+50	PPM
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		200	300	400	ps
PH_J	RMS Phase Jitter (random)	OUT2 = 106.25 MHz @ BW: 637 kHz to 10 MHz		–	1.6	–	ps
		OUT2 = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.5	–	ps
		OUT2 = 200 MHz @ BW: 1 MHz to 20MHz		–	0.7	–	ps
P_J	RMS Period Jitter	OUT2 = 106.25 MHz		–	1.8	2.3	ps
		OUT2 = 156.25 MHz		–	1.3	1.8	ps
		OUT2 = 200 MHz		–	1.3	1.8	ps

LVPECL, 2.5V ±10% ,-40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{sta}	Frequency Stability	nclusive of initial tolerance, operating temperature, rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	PPM
			-40 to 85°C	-50	–	+50	PPM
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		200	300	400	ps
PH_J	RMS Phase Jitter (random)	OUT2 = 106.25 MHz @ BW: 637 kHz to 10 MHz		–	1.6	–	ps
		OUT2 = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.5	–	ps
		OUT2 = 200 MHz @ BW: 1 MHz to 20MHz		–	0.7	–	ps
P_J	RMS Period Jitter	OUT2 = 106.25 MHz		–	1.8	2.3	ps
		OUT2 = 156.25 MHz		–	1.3	1.8	ps
		OUT2 = 200 MHz		–	1.3	1.8	ps

HCSL, 3.3V ±10% ,-40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{sta}	Frequency Stability	nclusive of initial tolerance, operating temperature, rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	PPM
			-40 to 85°C	-50	–	+50	PPM
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		300	450	550	ps
PH_J	RMS Phase Jitter (random)	OUT2 = 100 MHz @ BW: 1.5 MHz to 22 MHz		–	0.8	–	ps
		OUT2 = 200 MHz @ BW: 1.5 MHz to 22 MHz		–	0.4	–	ps
P_J	RMS Period Jitter	OUT2 = 100 MHz		–	1.6	2.2	ps
		OUT2 = 200 MHz		–	1.5	1.9	ps

HCSL, 2.5V ±10% ,-40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{sta}	Frequency Stability	nclusive of initial tolerance, operating temperature, rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	PPM
			-40 to 85°C	-50	–	+50	PPM
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		300	450	550	ps
PH_J	RMS Phase Jitter (random)	OUT2 = 100 MHz @ BW: 1.5 MHz to 22 MHz		–	0.8	–	ps
		OUT2 = 200 MHz @ BW: 1.5 MHz to 22 MHz		–	0.4	–	ps
P_J	RMS Period Jitter	OUT2 = 100 MHz		–	1.6	2.2	ps
		OUT2 = 200 MHz		–	1.5	2.1	ps

LVDS, 3.3V ±10% ,-40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{sta}	Frequency Stability	nclusive of initial tolerance, operating temperature, rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	PPM
			-40 to 85°C	-50	–	+50	PPM
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		200	300	450	ps
PH_J	RMS Phase Jitter (random)	OUT2 = 106.25 MHz @ BW: 637 kHz to 10 MHz		–	1.7	–	ps
		OUT2 = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.7	–	ps
		OUT2 = 200 MHz @ BW: 1 MHz to 20MHz		–	0.7	–	ps
P_J	RMS Period Jitter	OUT2 = 106.25 MHz		–	2.0	2.7	ps
		OUT2 = 156.25 MHz		–	1.8	2.5	ps
		OUT2 = 200 MHz		–	1.8	2.5	ps

LVDS, 2.5V ±10% ,-40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{sta}	Frequency Stability	nclusive of initial tolerance, operating temperature, rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	PPM
			-40 to 85°C	-50	–	+50	PPM
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		200	300	450	ps
PH_J	RMS Phase Jitter (random)	OUT2 = 106.25 MHz @ BW: 637 kHz to 10 MHz		–	1.7	–	ps
		OUT2 = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.7	–	ps
		OUT2 = 200 MHz @ BW: 1 MHz to 20MHz		–	0.7	–	ps
P_J	RMS Period Jitter	OUT2 = 106.25 MHz		–	2.5	3.3	ps
		OUT2 = 156.25 MHz		–	2.4	3.5	ps
		OUT2 = 200 MHz		–	2.4	3.5	ps

CML, 3.3V ±10% ,-40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{sta}	Frequency Stability	nclusive of initial tolerance, operating temperature, rated power supply voltage change, load change	0 to 70°C	-10	–	+10	PPM
			-20 to 70°C -40 to 85°C	-15	–	+15	PPM
				-20	–	+20	PPM
				-25		+25	PPM
				-50		+50	PPM
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		220	330	400	ps
PH_J	RMS Phase Jitter (random)	OUT2 = 106.25 MHz @ BW: 637 kHz to 10 MHz		–	1.6	–	ps
		OUT2 = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.6	–	ps
		OUT2 = 200 MHz @ BW: 1 MHz to 20MHz		–	0.8	–	ps
P_J	RMS Period Jitter	OUT2 = 106.25 MHz		–	2	2.5	ps
		OUT2 = 156.25 MHz		–	1.9	2.5	ps
		OUT2 = 200 MHz		–	1.9	2.4	ps

CML, 2.5V ± 10% ,-40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{sta}	Frequency Stability	nclusive of initial tolerance, operating temperature, rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	PPM
			-40 to 85°C	-50	–	+50	PPM
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		220	330	400	ps
PH_J	RMS Phase Jitter (random)	OUT2 = 106.25 MHz @ BW: 637 kHz to 10 MHz		–	1.6	–	ps
		OUT2 = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.6	–	ps
		OUT2 = 200 MHz @ BW: 1 MHz to 20MHz		–	0.8	–	ps
P_J	RMS Period Jitter	OUT2 = 106.25 MHz		–	2.1	2.5	ps
		OUT2 = 156.25 MHz		–	1.9	2.5	ps
		OUT2 = 200 MHz		–	1.9	2.5	ps

CML, 1.8V ± 5% ,-40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{sta}	Frequency Stability	nclusive of initial tolerance, operating temperature, rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	PPM
			-40 to 85°C	-50	–	+50	PPM
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		220	330	425	ps
PH_J	RMS Phase Jitter (random)	OUT2 = 106.25 MHz @ BW: 637 kHz to 10 MHz		–	1.7	–	ps
		OUT2 = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.6	–	ps
		OUT2 = 200 MHz @ BW: 1 MHz to 20MHz		–	0.8	–	ps
P_J	RMS Period Jitter	OUT2 = 106.25 MHz		–	2.3	2.9	ps
		OUT2 = 156.25 MHz		–	2.1	2.7	ps
		OUT2 = 200 MHz		–	2.1	2.7	ps

Termination Diagrams

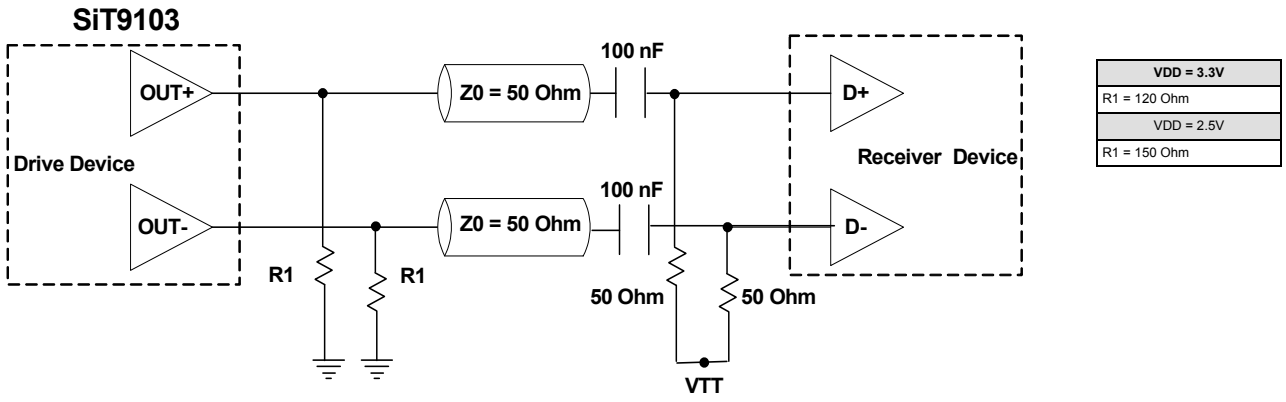


Figure 1. LVPECL AC Coupled Typical Termination

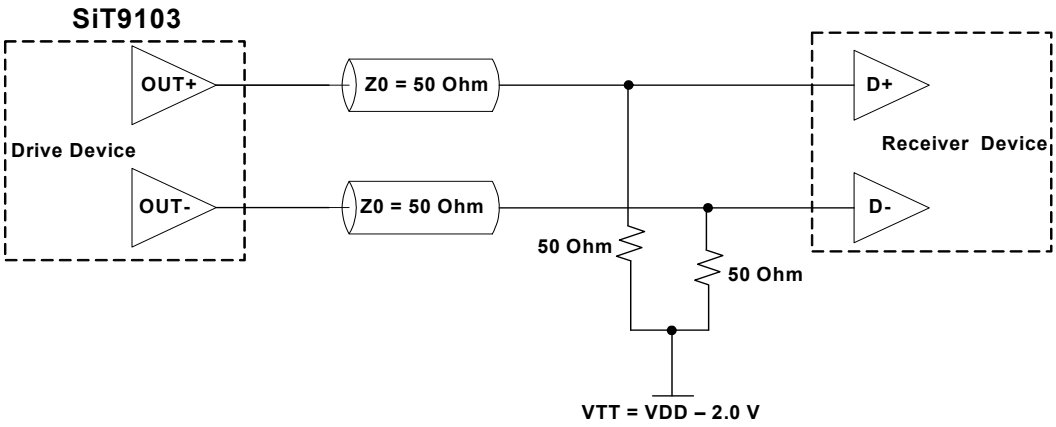


Figure 2. LVPECL DC Coupled Typical Termination with Termination Voltage

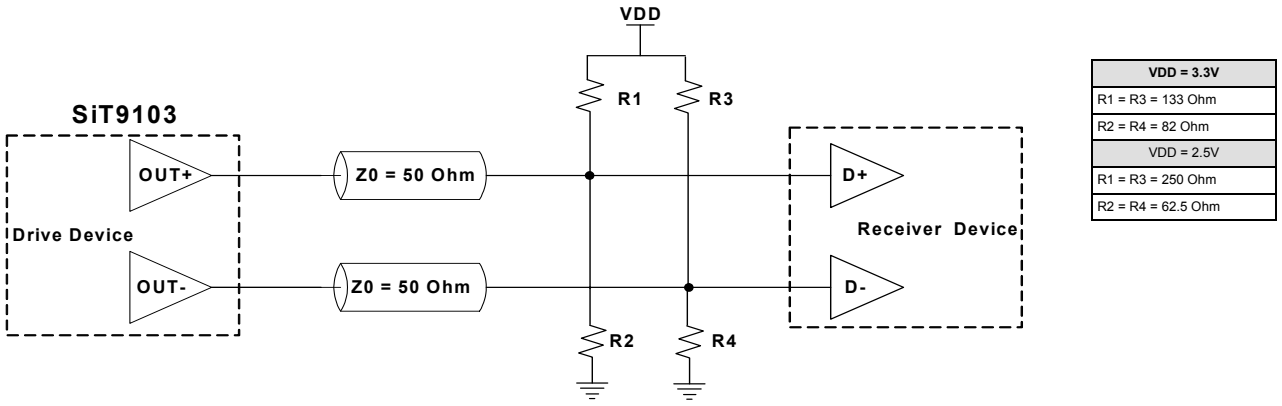


Figure 3. LVPECL DC Coupled Typical Termination without Termination Voltage

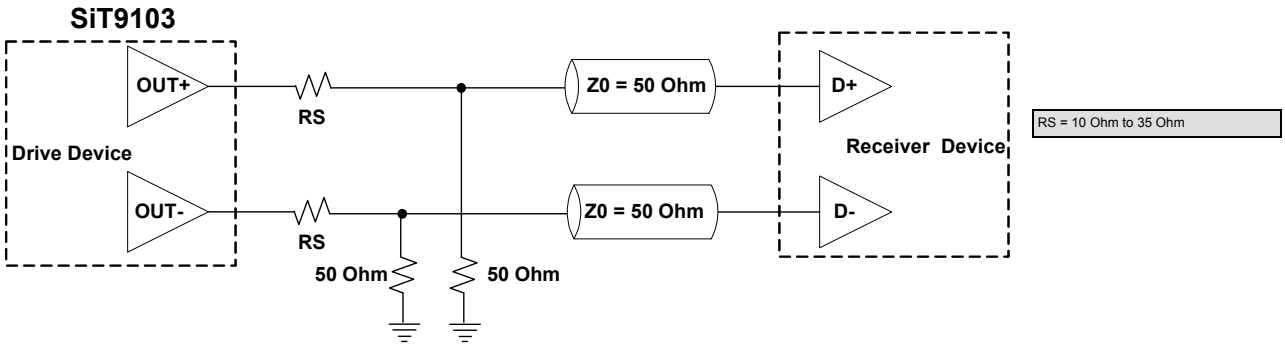


Figure 4. HCSL Typical Termination

Note:
1. All the tests are done with RS = 20 Ohm (recommended).

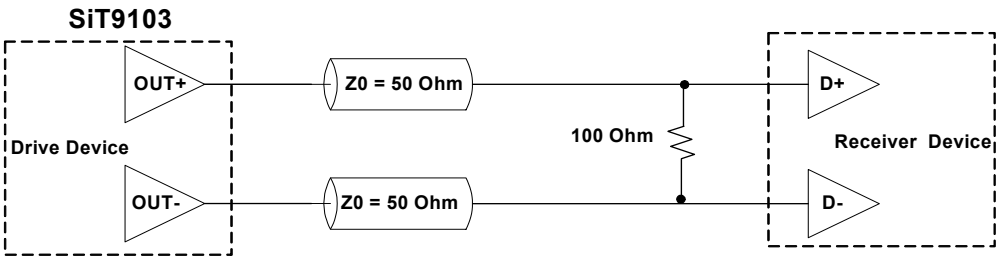
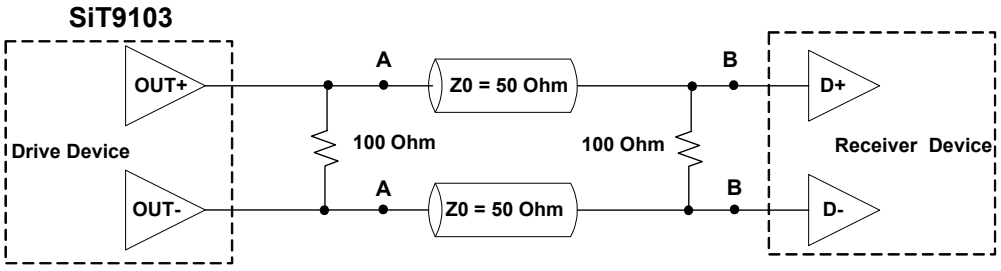
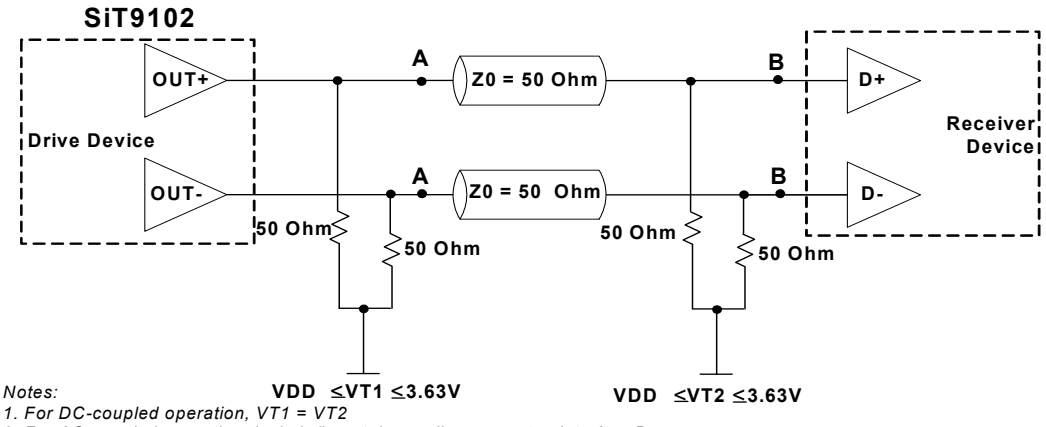


Figure 5. LVDS Single Termination (Load Terminated)



*Note: For AC coupled operation, include/insert decoupling caps at points **A** or **B***

Figure 6. LVDS Double Termination (Source + Load Terminated)



Notes:
1. For DC-coupled operation, VT1 = VT2
2. For AC coupled operation, include/insert decoupling caps at points A or B
2. For AC-coupled operation with capacitors placed at point A, VT2 sets the input common mode of Receiver Device and need not to be related to VT1

Figure 7. CML Double Load Termination

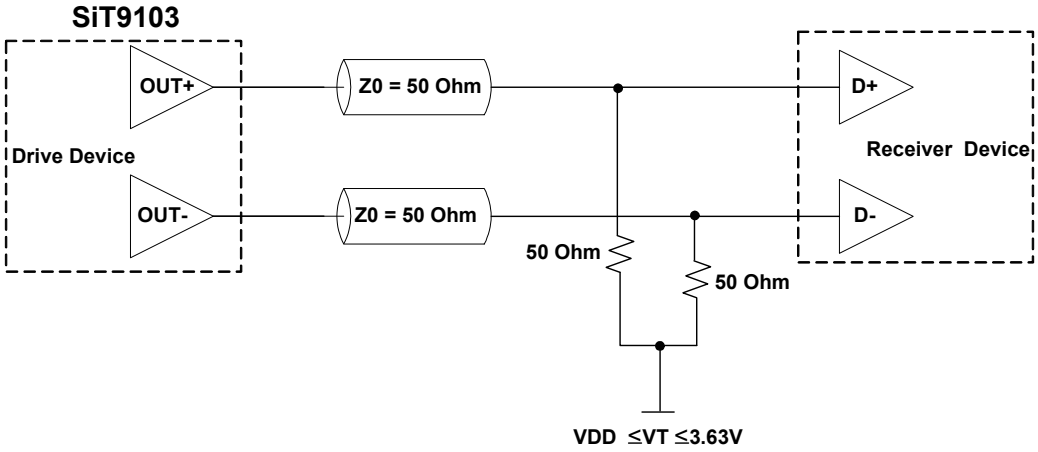
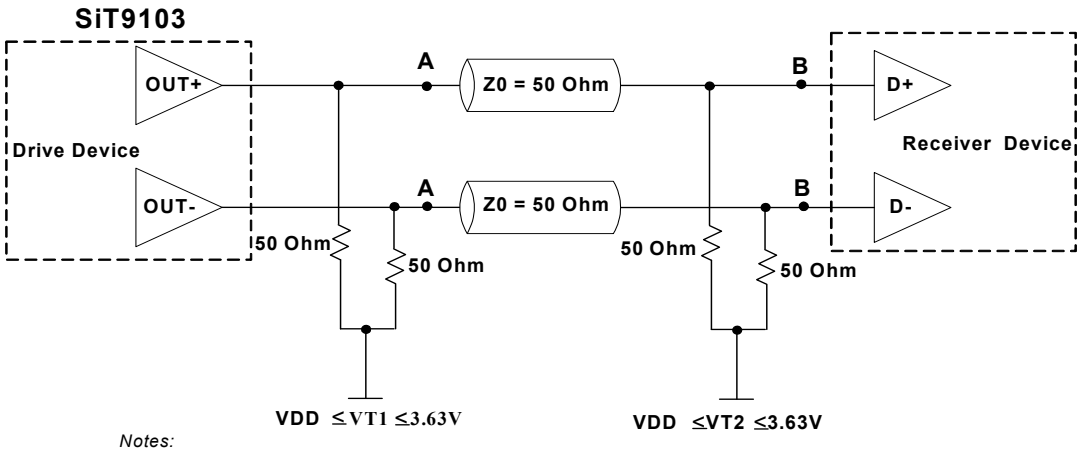


Figure 8. CML Single Load Termination



Notes:
1. For DC-coupled operation, VT1 = VT2
2. For AC-coupled operation, VT2 sets the input common mode of Receiver Device and need not to be related to VT1

Figure 9. CML Double Load Termination

Ordering Information[1]

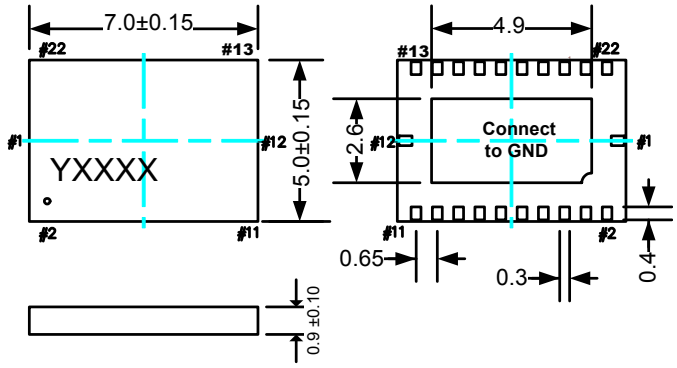
Part Number	Package Description	Freqiency Stability	Product Flow
SiT9103AC-2xxx	22-pin QFN	±25ppm	-20°C to 70°C
SiT9103AI-2xxx	22-pin QFN	±25ppm	-40°C to 85°C
SiT9103AC-3xxx	22-pin QFN	±50ppm	-20°C to 70°C
SiT9103AI-3xxx	22-pin QFN	±50ppm	-40°C to 85°C

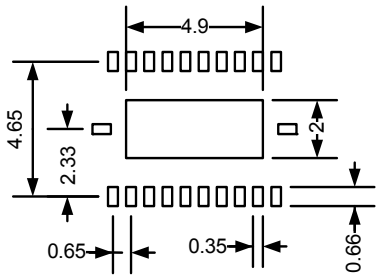
Package Information [2]

Dimension (mm)

Land Pattern [3](recommneded) **(mm)**

7.0 x 5.0 x 0.9mm





Notes:
1. "xxx" denotes the assigned product dash number.
2. "Y" denotes manufacturing origin and "XXXX" denotes manufacturing lot number. The value of "Y" depend on the assembly location of the device.
3. A capacitor of value 0.01µF between VDD and GND is recommended.